IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application: Alexander W. Hietala
Serial No.: 09/879,806 Examiner: TBA
Filed: 06/12/2001 Art Unit: TBA
For: FRACTIONAL-N DIGITAL MODULATION WITH ANALOG IQ INTERFACE

Commissioner for Patents
Washington, DC 20231

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

In accordance with 37 C.F.R. 1.56, counsel wishes to make of record the attached additional items of information for the Examiner's consideration in connection with this application. Also enclosed is a form PTO-1449 for the Examiner's convenience in making such consideration of record. Inclusion herein of any particular item of information is not to be construed as an admission that same is prior art.

The Director is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account 50-1732.

Respectfully submitted,

Benjamin S. Withrow
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Date: April 26, 2002
File No.: 2867-127

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CERTIFICATE OF MAILING

I HEREBY CERTIFY THAT THIS DOCUMENT IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST-CLASS MAIL, IN AN ENVELOPE ADDRESSED TO: **COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231**, ON 4/26/02 (Date of Deposit)

Name of Depositor Jennifer Rush Signature Jennifer Rush Date of Signature 4/26/02

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FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DKT NO. 2867-127	SERIAL NO. 09/879,806
		APPLICANT Alexander W. Hietala	
	INFORMATION DISCLOSURE STATEMENT BY APPLICANT	FILING DATE 6/12/2001	GROUP TBA

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CL.	SUBCL.	FILING DATE IF APPROP.
	A	3,538,450	11/1968	Andrea et al.	331	10	
	B	4,875,046	10/1989	Lewyn	341	148	
	C	5,117,206	05/1992	Imamura	331	158	
	D	5,235,335	08/1993	Hester et al.	341	172	
	E	5,493,715	02/1996	Humphreys et al.	455	264	
	F	5,973,633	10/1999	Hester	341	172	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CL.	SUBCL	TRANSLATION	
							YES	NO

OTHER DOCUMENTS (Incl. Author, Title, Date, Pertinent pages, etc.)

	G	Dunning et al., "An All-Digital Phase-Locked Loop with 50-Cycle Lock Time Suitable for High-Performance Microprocessors," IEEE Journal of Solid-State Circuits, Vol. 30, No. 4, April 1999, pages 412 -422.
	H	Kral et al., "RF-CMOS Oscillators with Switched Tuning," Proceedings of the IEEE 1998 Custom Integrated Circuits Conference, May 1998, pages 555-558.
	I	Miller, Brian and Conley, Robert J., "A Multiple Modulator Fractional Divider," IEEE Transactions on Instrumentation and Measurement, Vol. 40, No. 3, June 1991, pages 578-583.
	J	Wilson et al., "A CMOS Self-Calibrating Frequency Synthesizer," IEEE Journal of Solid-State Circuits, Vol. 35, No. 10, October 2000, pages 1437-1444.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.